MSI-P400

PC/104 QUADRATURE DECODER/COUNTER CARD

PC/104 Embedded
Industrial Analog I/O Series

Microcomputer Systems, Inc.
1814 Ryder Drive ¨ Baton Rouge, LA 70808
Ph (225)769-2154 ¨ Fax (225) 769-2155
http://www.microcomputersystems.com
Email: staff@microcomputersystems.com

DESCRIPTION

The MSI-P400 is a 15-channel quadrature decoder/counter PC/104 card designed for monitoring up to 15 quadrature encoder inputs used in monitoring motor shaft rotations. Each channel provides a 16-bit binary up/down counter with full 4X decoding using a Hewlett-Packard HCTL-2016 decoder IC. This device provides a digital noise filter network, 4X decoding logic, a 16-bit counter, and a 16-bit latched output. A card outline is shown in Figure 1.

Inputs from quadrature encoders are applied via a 40-pin input connector (J1) that requires a frequency and a reference signal input for each channel in use. Input signals are TTL levels. The clock employed for processing the input signals is derived from SYSCLK (6 to 8.33 MHz, depending on the processor card used) of the PC/104 bus. This clock signal is divided by 4 to provide the clock inputs to the HCTL-2016 decoder

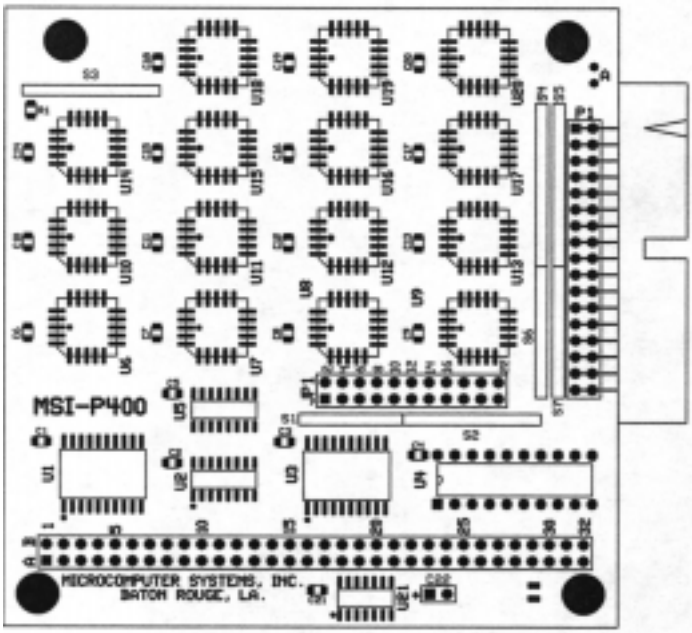

Figure 1. Outline of MSI-P400 Card.

The maximum frequency that can be applied to either a frequency or reference input is

$$f_{max} = SYSCLK/12$$

Therefore, for SYSCLK = 8.33 MHz, f_{max} = 694 KHz.

Each channel has a 16-bit up/down counter and an output latch. When the frequency input leads the reference input (nominally by 90 degrees), the counter counts up. Conversely, when the reference input leads the frequency input (nominally by 90 degrees), the counter counts down. Up counts are from 0 to 7FFF hexadecimal (0 to 32,767 decimal). Down counts are from FFFF to 8000 hexadecimal (-1 to -32,768 decimal). Roll-over occurs at the 0 and FFFF boundaries, of course, and the monitoring software must account for the roll-over event. A universal programmable reset is also provided to set all channel counts to zero.The card is an 8-bit stackthrough unit that requires +5V from the PC/104 bus.

Card Addressing

The I/O-mapped card address is set by installing appropriate jumpers on JP1, pins 1 thru 22. An uninstalled jumper for a given address bit sets the bit to 1 (true) and an installed jumper sets the bit to 0 (false). Addresses A5 thru A15 are jumper selectable for defining the *base address* of the card from 0000H to FFE0H on integral 20H boundaries, where H denotes a hexadecimal number. To assign a base address of 300H, for example, install all jumpers except JP1-15,16 (A8) and JP1-13,14 (A9).

Fifteen input channels, denoted as CH1 thru CH15, correspond to inputs FREQ1 and REF1 thru FREQ15 thru REF15, respectively. The I/O address of each channel is given in Table 1.

Count data is obtained by performing I/O reads at the addresses shown Table 1. An important issue in reading

Table 1. I/O Addresses of MSI-P400.

Channel	Low Byte of Count*	High Byte of Count*
CH1	base address+1	base address
CH2	base address+3	base address+2
CH3	base address+5	base address+4
CH4	base address+7	base address+6
CH5	base address+9	base address+8
CH6	base address+11	base address+10
CH7	base address+13	base address+12
CH8	base address+15	base address+14
CH9	base address+17	base address+16
CH10	base address+19	base address+18
CH11	base address+21	base address+20
CH12	base address+23	base address+22
CH13	base address+25	base address+24
CH14	base address+27	base address+26
CH15	base address+29	base address+28

* Offsets from the base address are in decimal notation.

the data is the validity of the data when a roll-over condition (0 to FFFF or 8000 to 7FFF) occurs during a read operation of the HCTL-2016 device. Although the device incorporates a latch and features inhibit logic to avoid an error in the event of this condition, it is not functional for the PC/104 bus transfer because the output enable (/OE, where / denotes complementation) of the device must remain valid (low) while reading both high and low bytes. Since the enables are driven by chip selects /CS0 thru /CS14 associated with bus address decoding for the byte data reads, the output enables of the HCTL-2016 become high after each read. This resets the inhibit logic of the HCTL-2016 following each byte read which defeats the inhibit logic function. **It is therefore recommended when reading a channel count that a high-byte read followed by a low-byte read followed by a high-byte read be performed until the high bytes of these consecutive reads are equal.** Please contact the MSI staff at (225) 769-2154 with any questions regarding the read operation.

Count Reset

The counts contained in all registers (high and low bytes) can be reset to zero by performing a write of any value to the base address. The decoding logic of the MSI-P400 performs a reset on all HCTL-2016 devices.

Input Connector Pin Assignments

Table 2. Input Connector J1.

Pin No.	Signal	Pin No.	Signal
1	FREQ1	2	REF1
3	FREQ2	4	REF2
5	FREQ3	6	REF3
7	FREQ4	8	REF4
9	Ground	10	FREQ5
11	REF5	12	FREQ6
13	REF6	14	FREQ7
15	REF7	16	FREQ8
17	REF8	18	Ground
19	FREQ9	20	REF9
21	FREQ10	22	REF10
23	FREQ11	24	REF11
25	FREQ12	26	REF12
27	Ground	28	FREQ13
29	REF13	30	FREQ14
31	REF14	32	FREQ15
33	REF15	34	Ground

MSI-P400 Circuit Diagram

Contact MSI personnel at 225-769-2154 for schematic diagrams.