VISION VL5430 Camera Module

Dual standard CMOS Camera Module with support for ADC and external control via serial interface

PRODUCT DATASHEET

DISTINCTIVE CHARACTERISTICS

- Complete Video Camera module, including lens
- EIA/CCIR standard compatible
- Low power operation (250mW Typical)
- Integral 75Ω video driver
- Frame & line timing signals for external ADC
- Optional image output in four quarters, with output driver tristate option for multiplexing
- Automatic Exposure and Gain Control
- Automatic Black Level Calibration
- Linear or Gamma corrected output option
- Control options selectable with on board links
- External control/configuration via serial interface

GENERAL DESCRIPTION

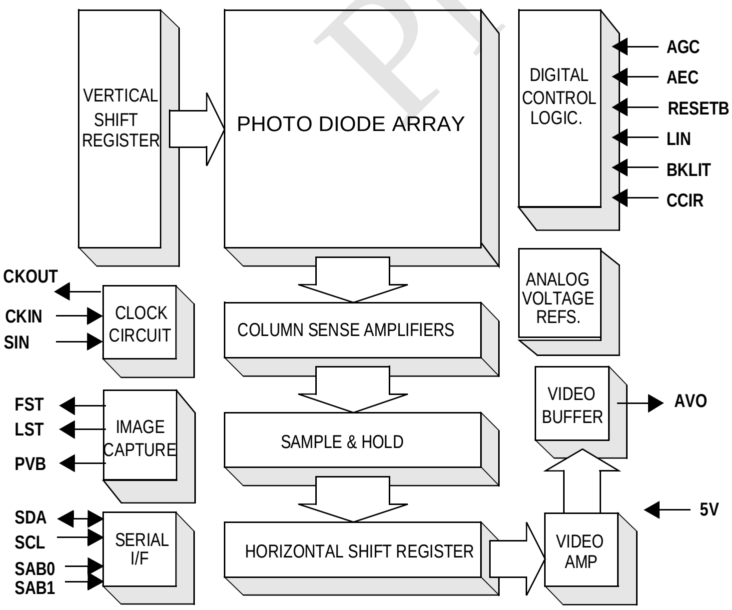
The VL5430 is a complete video camera system based on VISION's highly-integrated VLSI sensor device, the VV5430. The module is suitable for applications requiring minimum external circuitry, digitisation of the video signal or external microprocessor control.

The device incorporates a 388 x 295 pixel image sensor and all the necessary support circuits to generate composite video into a 75Ω load. Additional control signals support pixel locked digitisation of the video signal.

A bi-directional serial interface and internal register set allow full control and monitoring of all camera functions. Automatic control of exposure, gain and black level give a wide range of operating conditions. All major control functions are pin selectable giving maximum flexibility with ease of use.

The module is supplied as standard mounted with a narrow angle lens option — a complete camera system ideally suited for integration into digital imaging systems

BLOCK DIAGRAM



Pixel Format	384 x 287 (CCIR) 320 x 243 (EIA)
Pixel Size	12µm x 12µm
Array Size	4.66mm x 3.54mm
Min. illumination	0.5 lux (Standard Clock)
S/N	Typically 52dB
Exposure control	Automatic (to 146000:1)
Gain Control	Up to +20dB
Power Supply	5v ±5%
Power	< 300 mW
Temperature	0^oC - 40^oC

Contents

MAIN FEATURES

The VL5430 delivers a fully-formatted composite monochrome video signal. Standards options are EIA (320 x 244) and CCIR (384 x 287). On chip signal conditioning allows selection of linear or gamma-corrected output.

Different operational modes can be selected dynamically via the external interface or configured at power up by tying the appropriate pins. Extensive use of automated operation and on chip references means that only a small number of passive components are needed to realise a complete video camera.

Video Output

The integrated 75Ω driver eliminates the need for additional active components to drive standard loads, including double terminated lines.

The video signal can also be inhibited by setting the output to a high impedance state ('Tristated'), which enables multiplexing of a number of different sensors. This, together with vertical and horizontal 'shuffle' modes, means that four sensor images can be shown simultaneously on one display.

Frame, line and pixel timing signals are provided to facilitate pixel locked digitisation of the analog video data. In addition to the these outputs a synchronisation input (SIN) is also provided to allow the start of frame to be synchronised to an external event.

Automatic Exposure and Gain Control

The VV5430 features automatic exposure control that allows a single fixed-aperture lens to be used, and incorporates Normal and Backlit modes to give operation over a wide range of scene types. The system clock frequency can also be reduced to provide increased sensitivity.

Serial Interface

A bi-directional serial interface allows an external controller to set operational parameters and control exposure and gain values directly. The host can also interrogate VV5430 via the serial interface to determine the camera's operating modes and current state. This allows alternative automatic exposure and other control algorithms to be run in an external controller if the integrated versions are not suitable.

The VV5430 receives and transmits control and parametric data via a full duplex, two-wire serial interface. The host is communications master, with the camera either a slave receiver or transmitter. Messages consist of either three or five bytes of 8-bit data, with a maximum serial clock frequency of 100kHz. Since the serial clock is generated by the host, the host determines the data transfer rate.

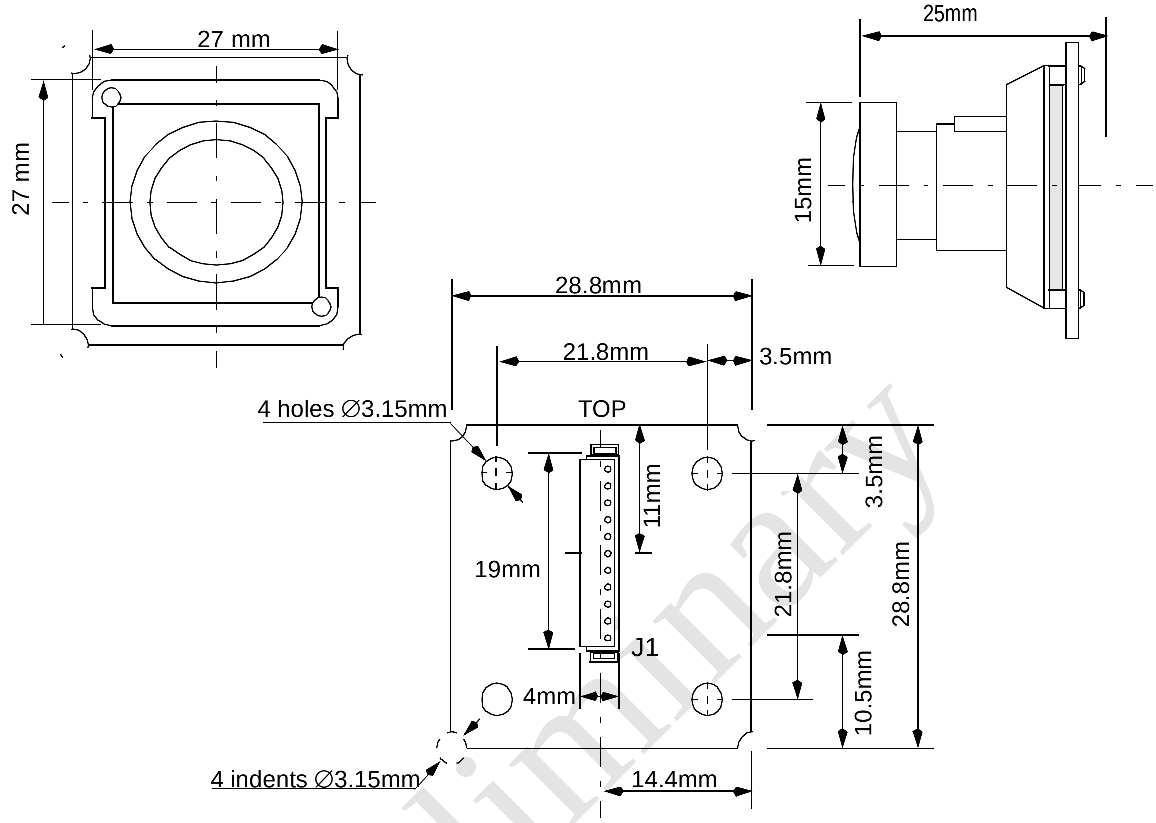
Option Part Numbers

Function	VISION Order Number
CCIR Video Output, 14.7456Mhz clock	VL5430S001
EIA Video Output, 12.000Mhz clock	VL5430S002

Note: All modules are supplied complete with narrow angle (4.3mm) lens; factory default settings are: AGC ON; AEC ON; Gamma Correction; SAB0 & SAB1 set to zero.

SPECIFICATIONS

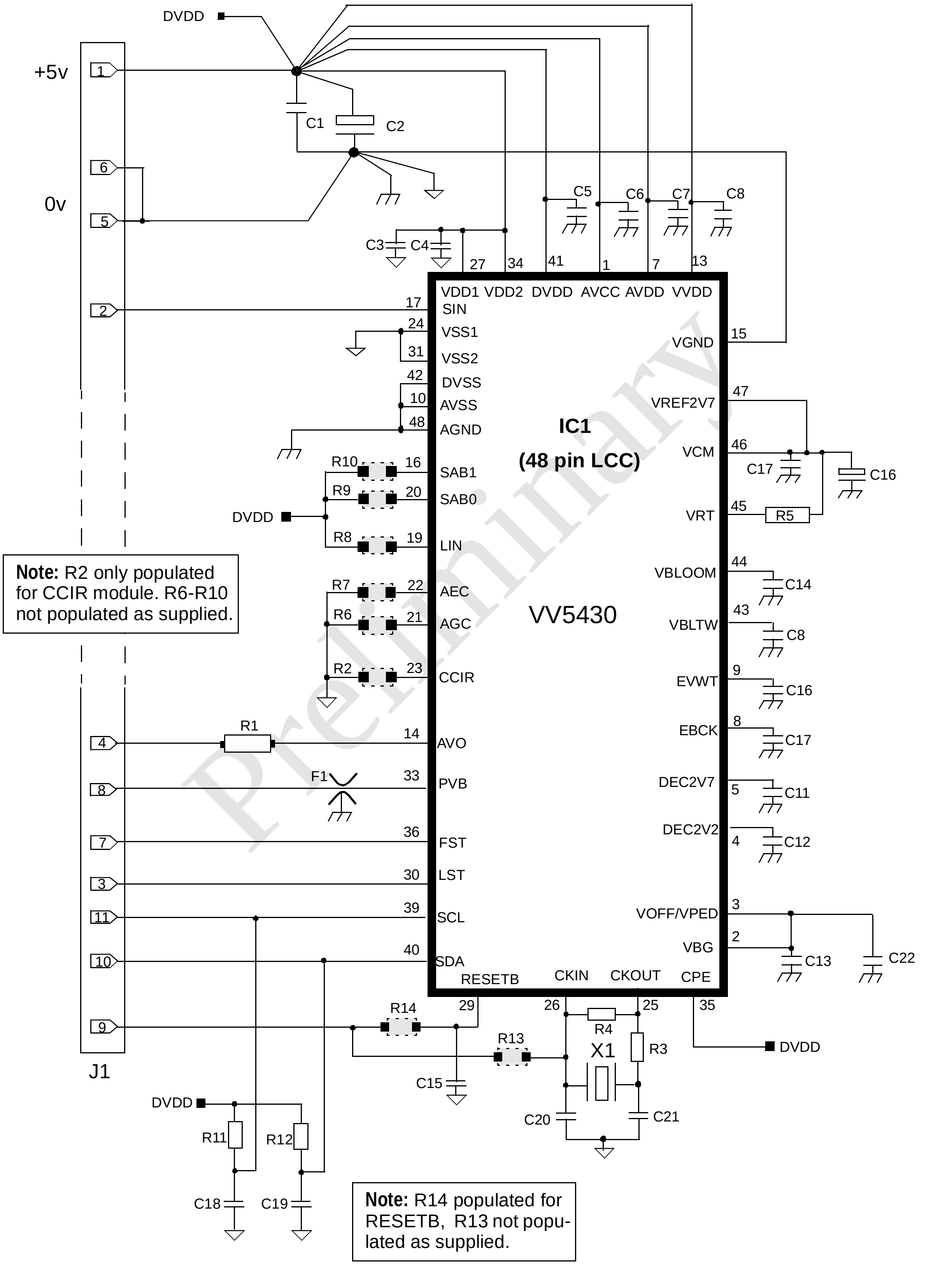
Package Details



Connector J1 Pinout

Pin	Function	Comments
1	+5 V Power	Power input - must be regulated externally to ± 5%
2	SIN	SIN - timing reset
3	LST	Line STart signal
4	AVO	Video Out - Terminate with 75R
5&6	Ground	Power and signal reference
7	FST	Frame STart signal
8	PVB	Pixel Valid Bar
9	Reset/CLK	Resets all systems to power-on states or drives internal clock ccts. (depends on R13/R14)
10	SDA	Serial DAta - bidirectional, open drain
11	SCL	Serial data CLock - must be generated by comms. host (up to 100KHz)

Module Schematic



Components shown with dotted outlines are empty sites on the PCB. These may be populated to change device function.

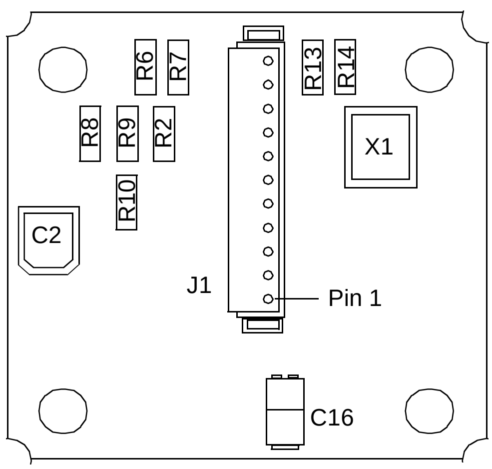
Parts List

Circuit Reference	Description	Value	Comments
C1, C3-C12, C14, C17, C22, C23	Ceramic Cap 0603 16V/20%	100nF	
C2	Aluminium Cap 6.3V 20%	1000µF	
C13	Ceramic Cap 0603 50V/10%	10nF	
C15, C18, C19	Ceramic Cap 0603 50V/5%	220pF	
C16	Tantalum Cap 16V20%	4.7uF	Case A
C20, C21	Ceramic Cap 0603 50V/5%	47pF	
R6-R10, R13	Resistor 0603 5%	0R	Not populated on PCB; may be used to select options.
R1	Resistor 0603 5%	75R	Video termination impedance
R2	Resistor 0603 5%	0R	Only fitted for EIA module
R3	Resistor 0603 5%	510R	
R4	Resistor 0603 5%	1M	
R5	Resistor 0603 5%	33R	
R11,R12	Resistor 0603 5%	2K2	
R14	Resistor 0603 5%	0R	J1-9 to RESETB (Default)
F1	EMI suppression filter		
X1	Resonator	12.00 MHz	Fitted for EIA module
X1	Resonator	14.74 MHz	Fitted for CCIR module
IC1	Image Sensor	VV5430	48LCC

On Board Option Selection

There is provision on the PCB for the user to change the power up condition of some of the internal registers by populating resistor sites with 0Ω 0603 resistors. Resistor R2 is factory-fitted for the standard EIA module, and R14 (which MUST be mutually exclusive with R13) is fitted to connect J1-9 to RESETB; standard modules are supplied with all other sites unpopulated.

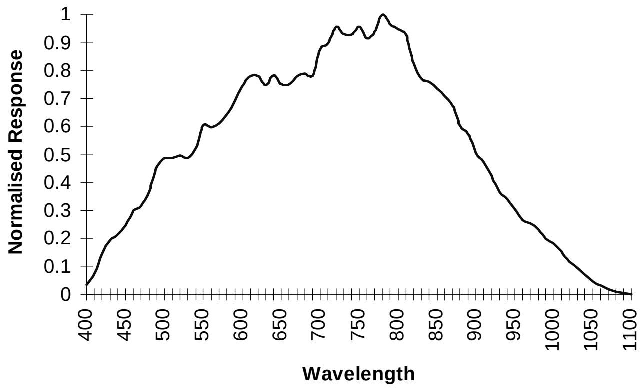
NOTE: Conditions set in this way cannot be overridden by the serial interface.



Site	Unpopulated	Populated
R2	CCIR Mode	EIA Mode
R6	AEC On	AEC Off
R7	AGC On	AGC Off
R8	Gamma Mode	Linear Mode
R9	SAB0 = 0	SAB0 = 1
R10	SAB1 = 0	SAB1 = 1
R13*	Default (R14 fitted)	J1-9 = CKIN
R14*	When R13 fitted	J1-9 = RESETB

*Note: R13 & R14 must not be fitted together.

Spectral Response



Lens

The VL5430 is supplied fitted with a narrow angle lens mounted in a plastic holder, the optical specification of which is shown below:

Characteristic	Narrow Angle
Horizontal Field of View	61°
Vertical Field of View	46°
Relative aperture	1:1.8
Resolution	>80 cycles/mm on axis
Distortion	<8.5% (TV distortion)
Operating wavelength	350nm to 750nm

Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5 to +7.0 volts
Voltage on other input pins	-0.5 to V_{DD} + 0.5 volts
Temperature under bias	-15°C to 85°C
Storage Temperature	-30°C to 125°C
Maximum DC TTL output Current Magnitude	10mA (per o/p, one at a time, 1sec. duration)

Note: Exceeding the Absolute Maximum Ratings may induce failure; prolonged exposure to maximum ratings may reduce reliability. Functionality at or above these conditions is not implied.

DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{DD}	Operating supply voltage	4.75	5.0	5.25	Volts	
V_{IH}	Input Voltage Logic "1"	2.4		V_{DD}+0.5	Volts	
V_{IL}	Input Voltage Logic "0"	-0.5		0.8	Volts	
T_A	Ambient Operating Temperature	0		70	^oC	Still air

AC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
CKIN	EIA Crystal frequency		12.0000		MHz	1
CKIN	CCIR Crystal frequency		14.7456		MHz	1
SCL	Serial Data Clock			100	KHz	2

1. Pixel Clock = $^{CKIN}/_2$
2. Serial Interface clock must be generated by host processor.

Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
I_{DCC}	Digital supply current		10		mA	1
I_{ADD}	Analog supply current		25		mA	1
I_{DD}	Overall supply current		35		mA	1
V_{REF2V7}	Internal voltage reference		2.700		Volts	
V_{BG}	Internal bandgap reference		1.22		Volts	
V_{OH}	Output Voltage Logic "1"	2.4			Volts	I_{OH} = 2mA
V_{OL}	Output Voltage Logic "0"			0.6	Volts	I_{OL} = -2mA
I_{ILK}	Input Leakage current	-1			µA	V_{IH} on input
				1	µA	V_{IL} on input

Typical conditions, V_{DD} = 5.0 V, T_A = 27^{o}C

1. Digital and Analogue outputs unloaded - add output current.

Operating Characteristics

Parameter	min.	typ.	max.	units	Note
Dark Current Signal		50		mV/Sec	Modal pixel voltage due to photodiode leakage under zero illumination with Gain=1 (V_{dark} = (V_{t1} - V_{t2})/(t1-t2), calculated over two different frames
Sensitivity		6		V/Lux·Sec	V_{Ave}/Lux·10ms, where Lux gives 50% saturation with Gain=1 and Exposure=10ms
Min. Illumination		0.5		Lux	Standard CCIR clock
Shading		TBA		%	Variance of V_{ave} over eight equal blocks at 66% saturation level illumination
Random Noise		-52		dB	RMS variance of all pixels, at 66% saturation, over four frames
Smear		TBA		%	Ratio of V_{ave} of the area outside a rectangle 25 lines high illuminated at 500x$V_{50\%}$ level to V_{Ave} of the rectangle
Flicker		TBA		%	Variation of V_{ave} of one line from field to field at 66% saturation level illumination
Lag		TBA		%	Average residual signal with no illumination in the field following one field of 66% sat. illumination
Blooming		TBA			Ratio of spot illumination level that produces 0.1xV_{sat} output from immediately around the spot to the V_{sat} spot illumination level (pinhole target)

Note: Devices are normaly not 100% tested for the above characterisation parameters, other than Dark Current Signal (see Blemish Specification below).

All voltage (V_A, V_{ave}, V_{sat}, $V_{xx\%}$) measurements are referenced to the black level, V_{black}, and spot blemishes are excluded (see Blemish Specification below). $V_{xx\%}$ refers to the output that is xx% of saturation, that is peak white. .

Test Conditions

The sensor is tested using the example support circuit illustrated later in this document. Standard imaging conditions used for optical tests employ a tungsten halogen lamp to uniformly illuminate the sensor (to better than 0.5%), or to illuminate specific areas. A neutral density filter is used to control the level of illumination where required.

Illumination Colour Temp.	3200^{o} K
Clock Frequency	Std. CCIR
Exposure	Maximum
Gain	x1
Auto. Gain Control (AGC)	Off
Correction mode	Linear

Blemish Specification

A Blemish is an area of pixels that produces output significantly different from its surrounding pixels for the same illumination level. The definition of a Blemish Pixel varies according to testing conditions as follows:

Test	Exposure	Illumination	Blemish Pixel output definition
1 - Black Frame	Minimum	Black	Differing more than ± 100 mV. from modal value.
2 - Dark Current	Maximum	Black	Output more than three times the modal value (see Dark Current Signal above).
3 - Pixel Variation	Mid range	66% Sat.	Differing more than ±35mV from modal value. Note: The mode of pixel values must be within ±70 mV of 66% of V_{sat} for all devices.

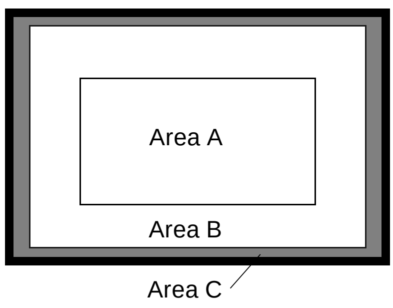
Note: Gain is set to Minimum and Correction set to Linear for all tests; measurement of blemishes for Test 3 is conducted under standard illumination (see above), set to produce average output of 66% saturation level.

The pixel area of the sensor is divided into the following areas to qualify the blemish specification:

Area A is the central area of the array as defined by the box with sides 50% of the linear height and 50% of the linear width of the array.

Area C is 10 vertical pixels by 10 horizontal pixels around the edge of the array.

Area B is the remaining area of the array.



The blemish specification is then defined as follows:

Image Area	Max. No. of Blemishes	Notes
Area A	0	No defects are allowed
Area B	4	Unconnected single pixels
	1	Of up to four connected pixels (2x2 max.)
Area C	Any number	Blemishes in this area are not significant, but the device shall, however, have no row or column (>50% of row or column) faults in any area.

VIDEO STANDARDS

The VV5430 has 2 different video format modes, producing CCIR or EIA standard composite Monochrome video output. Line standards and frequencies are as follows:

Video Mode	Format	Image (Pixels)	Crystal Frequency	CCIR pin
CCIR	4:3	384 x 287	14.7456 MHz	1
EIA	4:3	320 x 243	12.0000 MHz	0

VV5430 Video Modes

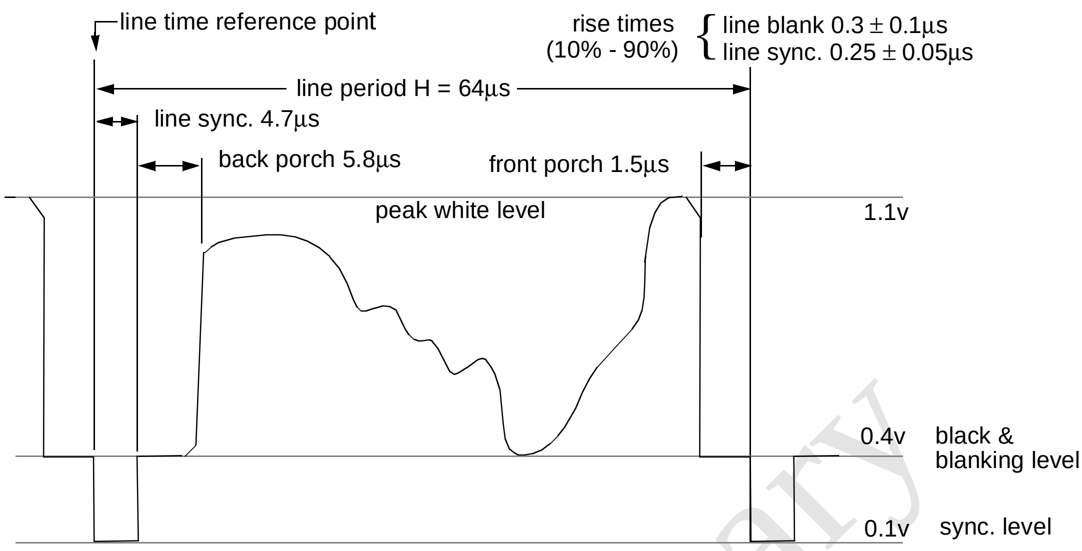
Video signal Characteristics

The following table summarises the composite video output levels (AVO) for the two standards, which are graphically illustrated on the following pages:

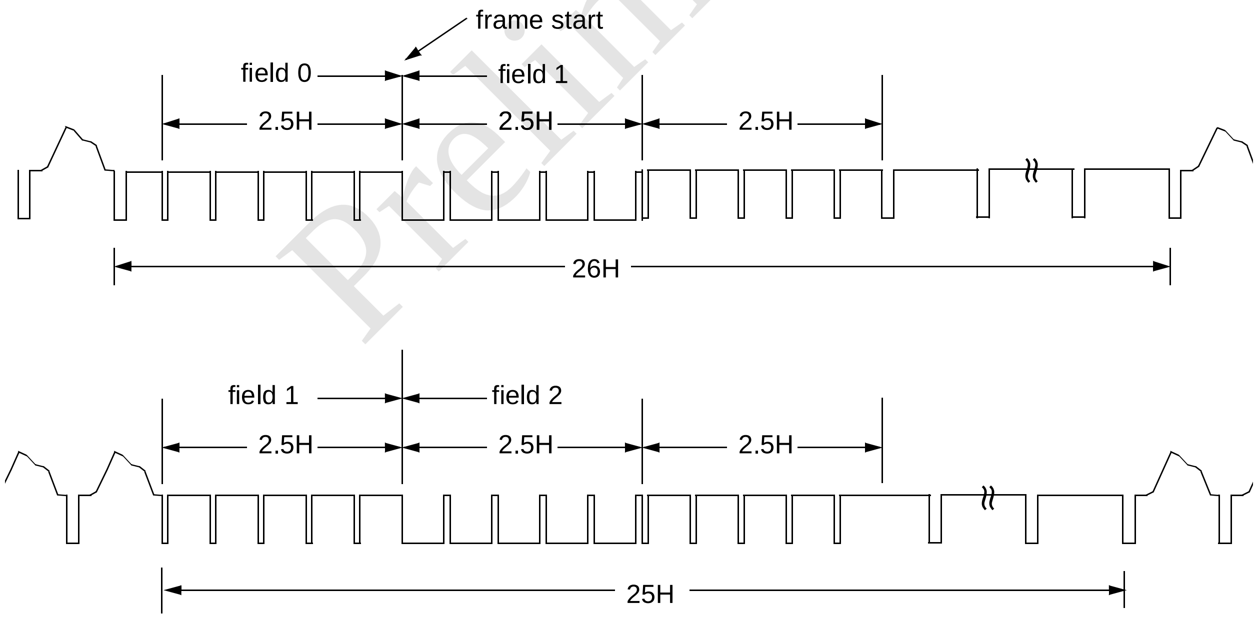
Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{Sync}	CCIR, EIA Sync. level		0.1		V	
V_{blank}	CCIR, EIA Blanking level		0.4		V	DC reference level
V_{black}	CCIR Black level		0.4		V	
	EIA Black level		0.5		V	
V_{Sat}	CCIR Saturation level		1.1		V	Peak White; AVO clipped at this level
	EIA Saturation level		1.2		V	

Note: All measurements are made with AVO driving one 75Ω load.

CCIR Timing Diagram

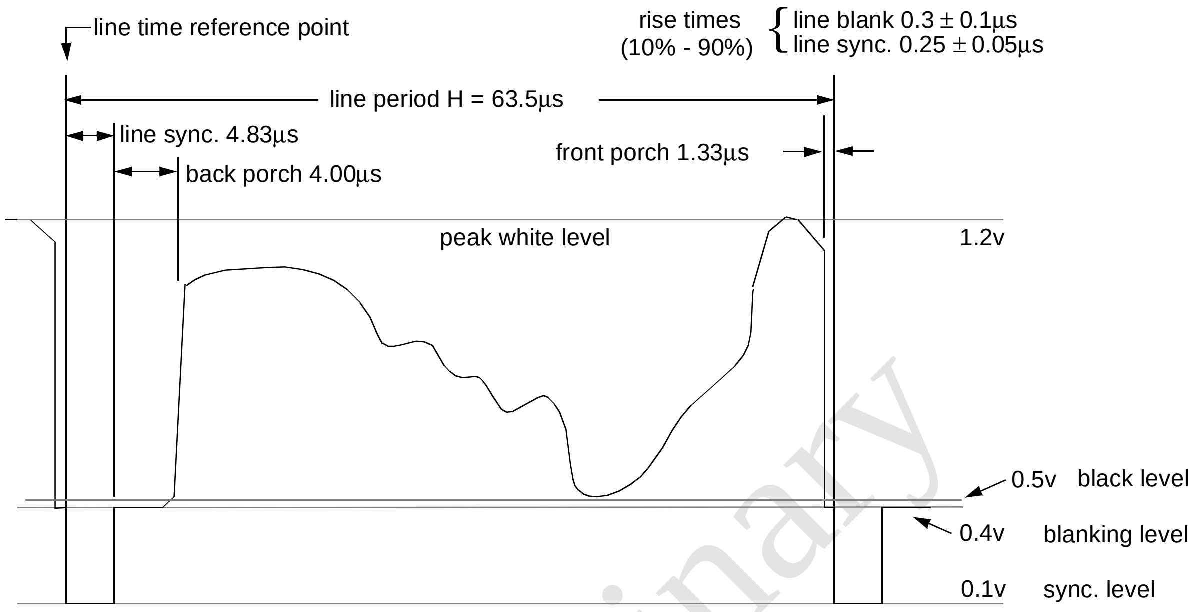


CCIR composite video signal - line level timing

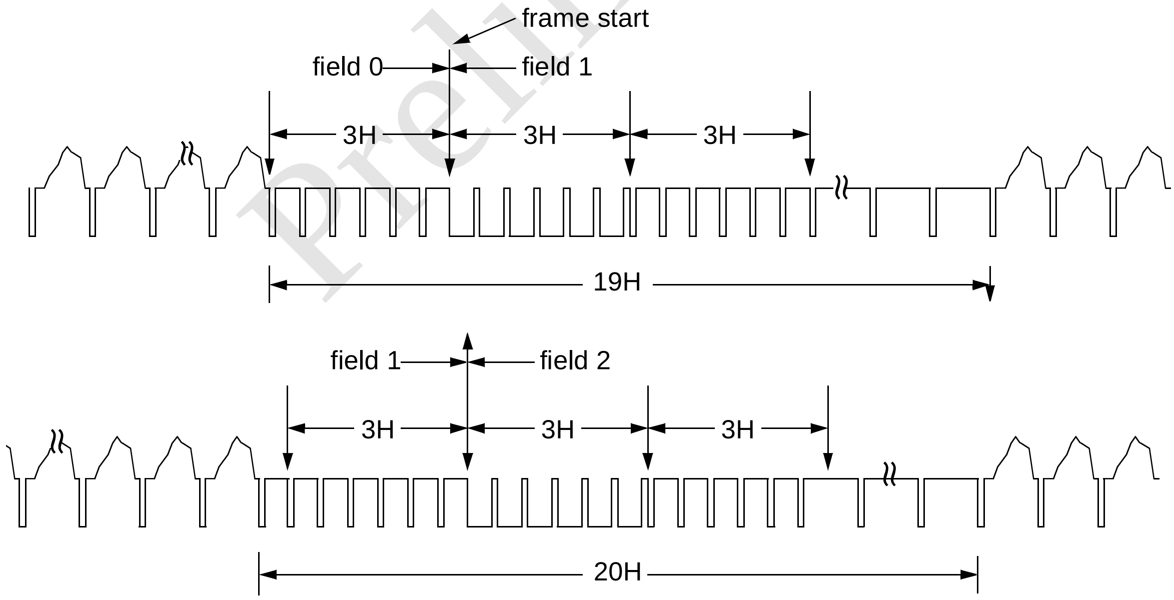


CCIR composite video signal - field level timing

EIA Timing Diagrams



EIA composite video signal - line level timing



EIA composite video signal - field level timing

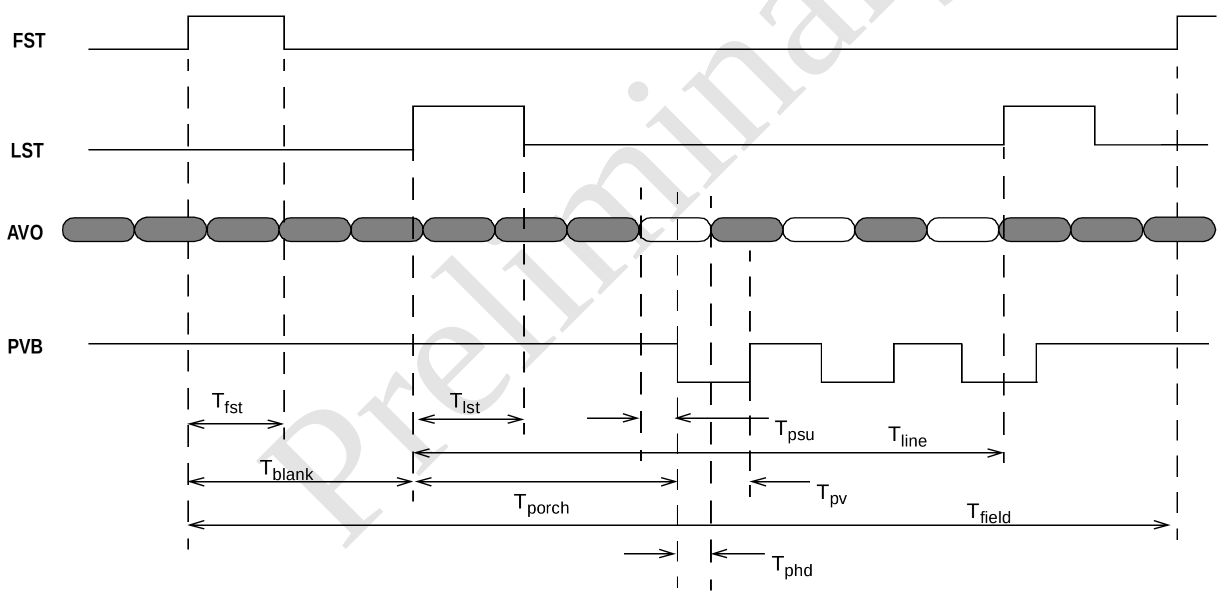
CONTROL SIGNALS FOR IMAGE DIGITISATION

The VV5430 camera can be used with an Analog-to-Digital Converter (ADC) and the necessary logic to form an image capture and processing system. The camera provides an analogue video output together with digital signals to qualify this output and synchronise image capture.

The signals provided for image capture are the following:-

- PVB: (Pixel Valid Bar) Complementary signals, their leading edges qualify valid pixel levels.
- LST: (Line STart) The rising edge signals the start of a visible line.
- FST: (Field STart) The rising edge signals the start of a field.

The following diagram illustrates the relative timing of the image capture signals. Scale is not actual but edge succession is preserved.



Frame Capture signal timing

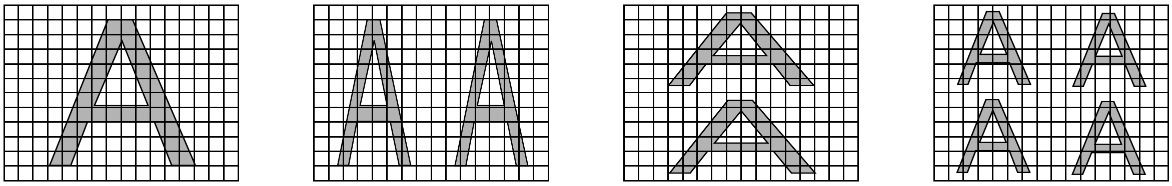
Image Capture Control Signal Timing

The time intervals given are correct for the recommended crystals:

Name	CCIR	EIA
Crystal Frequency (F_{CKIN})	14.7456 MHz	12.0000 MHz
Pixel clock period ($T_{pck} = 2/F_{CKIN}$)	135.63 nsec	166.67nsec
PVB (Pixel clock) mark:space	1:1	1:1
PVB low period ($T_{pvb} = T_{pck}/2$)	67.82 nsec	83.34 nsec
Even (first) field period (T_{field})	20.032 msec (313 x T_{line})	16.7005 msec (263 x T_{line})
Odd (second) field period (T_{field})	19.968 msec (312 x T_{line})	16.637 msec (262 x T_{line})
FST duration (T_{FST})	7.73 µsec (57 x T_{pck})	6.1 µsec (45 x T_{pck})
Line period (T_{line})	64.0 usec (472 x T_{pck})	63.5 µsec (381 x T_{pck})
LST duration (T_{LST})	4.61 µsec (34 x T_{pck})	4.66 µsec (28 x T_{pck})
First visible line delay (T_{blank})	704.949 µsec (11xT_{line} + 7xTpck)	762.833µsec (12xT_{line} + T_{pck})
First visible pixel delay (T_{porch})	10.58 µsec (78 x T_{pck})	8.833 µsec (53 x T_{pck})
Visible line period	52.083 µsec (384 x T_{pck})	53.333 µsec (320 x T_{pck})
Max AVO to PVB setup time (T_{psu})	33.9 nsec	41.7nsec
Min. PVB to AVO hold time (T_{phd})	30nsec	40nsec

SHUFFLE MODES

The pixels in the VV5430 sensor array can be output to AVO as alternate columns and rows by setting bits 5 and 6 in the Setup Code_1 register (header code 0001 - see Serial Interface for details). This has the effect of generating two, or four, identical low resolution images in one field:



Unshuffled Image — Horizontal Shuffle — Vertical Shuffle — Hor. + Vert. Shuffle

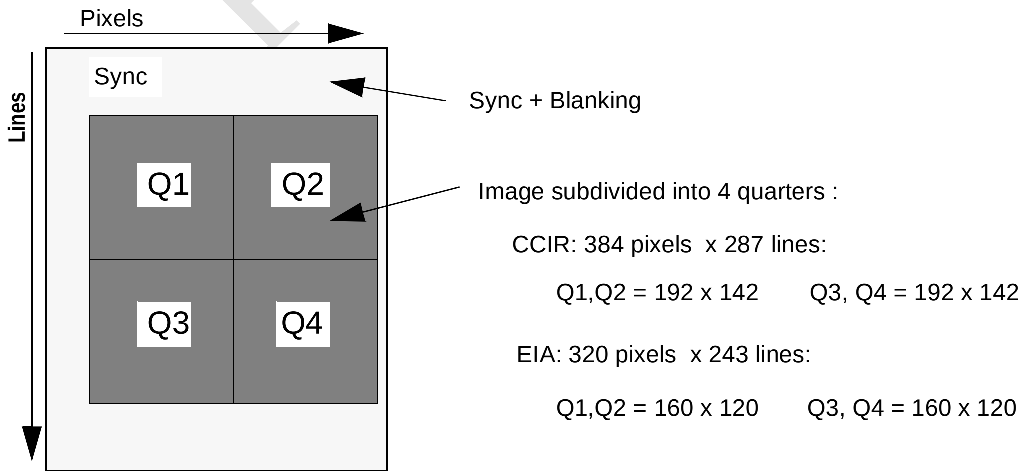
When this facility is combined with AVO Enable selected for the appropriate quarter, it is possible to display the images from four separate cameras on one monitor.

In order to achieve four identical images in one frame (from one sensor), bits 5 and 6 of Setup Code_1 must both be set via the serial interface, that is HSHUFFLE=1 and VSHUFFLE=1. The former interleaves odd and even pixel lines in the image, and the latter interleaves pixel columns. OE[0..2] can then Enable AVO output for any one quarter of the display field.

Quarter mode output

The VV5430 video output can be Enabled in different parts of the standard field by programming bits 9..11 of Setup Code_2, that is CE[0..2]; when not enabled, the AVO output is Tristated, that is floating at high impedance. Thus, a number of different sensor AVO outputs can be connected together and selectively enabled. This feature, together with bus addressing of up to four VV5430s on one serial link, is intended for multi-sensor systems that, in conjunction with bits 5,6 of Setup Code_1, enable the images from up to four cameras to be displayed on a single monitor.

By programming CE[0..2] different areas of the field can be enabled:.



The effect of OE[0..2] on AVO output is summarised in the following table:

:

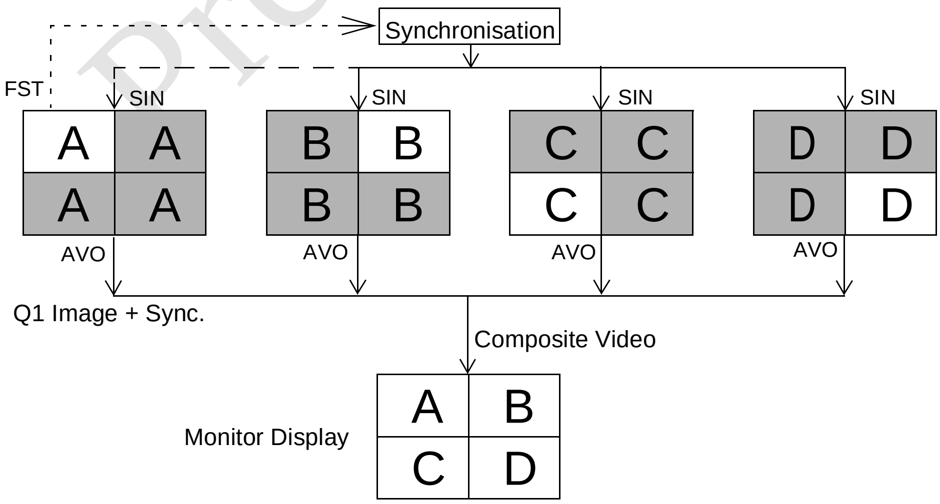
OE[2]	OE[1]	OE[0]	Regions where AVO is enabled
0	0	0	All (Normal operation)
0	0	1	None (AVO permanently tristate)
0	1	0	Sync only
0	1	1	Sync plus Q1 image
1	0	0	Q1
1	0	1	Q2
1	1	0	Q3
1	1	1	Q4

AVO Enable selection

Since each of the horizontal 'halves' of the frame is only 142 lines (CCIR) or 120 lines (EIA), there is a 'black band' of three lines separating the top half from the bottom half. Similarly, for timing purposes, there is a two pixel vertical black band separating the left and right halves of the frame. (See the timing diagram below.)

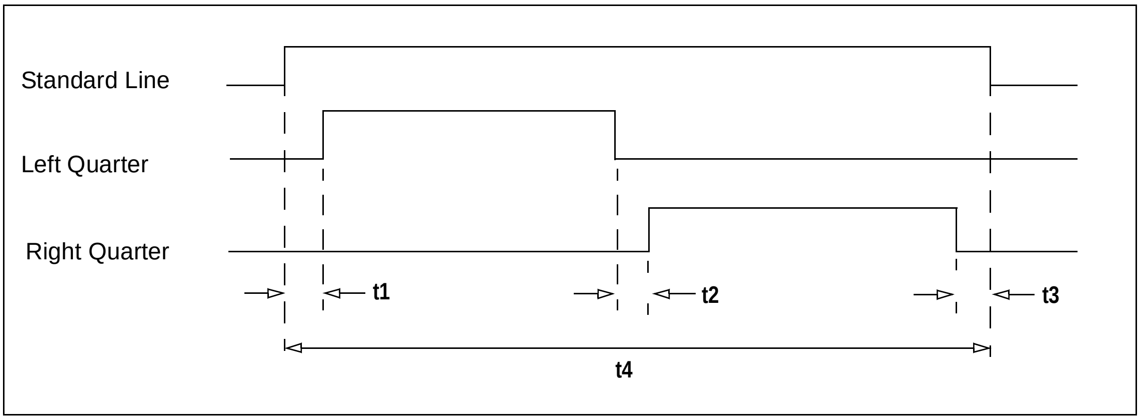
Multiplexing four cameras

Using the quarter mode of operation, it is possible, therefore, to combine the outputs of four separate VL5430 cameras (with appropriate control logic) and display four half resolution images on one monitor:



Note: One VL5430 camera would normally be used as 'master', and provide the Sync-plus-Q1 output for the monitor or other video device. A synch. signal, at frame frequency, is required via SIN (pin CN1-2) to keep the four cameras in step. This signal can be derived from the master camera FST output (with 'SNO Enable' set via Setup Code_3 bit 6), or be generated externally.

Quarter mode line timing.



Pixel timings for AVO 1/4 Mode:

Description	#t	CCIR		EIA	
		pck cycles	Time (us)	pck cycles	Time (us)
Left quarter Line Delay	t1	1	0.1356	1	0.1667
Duration of left quarter line		190	25.4928	158	26.0052
Inter-quarter Interval	t2	2	0.2713	2	0.3333
Duration of right quarter line		190	25.4928	158	26.0052
Right quarter border	t3	1	0.1356	1	0.1667
Duration of standard SI	t4	384	52.0704	320	53.3440

In addition there are line level signals to identify the top and bottom half of the active video area of the field: .

Description	Start line		Number of lines	
	CCIR	EIA	CCIR	EIA
Top half of field	First active line	First active line	142	120
Bottom half of field	Active line 145	Active line 124	142	120

There is a ‘black band’ of three video lines between the valid lines in the top half of the field and the valid lines in the bottom half of the field. This ensures that both halves of the field are the same size and provides a horizontal frame line. The line level timing described above also provides a two pixel vertical black line, hence the four quarters appear to be ‘framed’ in the display.

EXPOSURE CONTROL

Automatic exposure and gain control ensure operation of the VL5430 over a wide range of lighting conditions. Automatic black level control and optional 'Backlit' mode further ensure consistent picture quality. The VV5430 sensor controls exposure over a range of 99,000:1 in EIA mode and 146,000:1 in CCIR mode, and operates at illumination levels as low as 0.5 lux.

Note: The System Clock can be divided by up to eight times to further increase sensitivity by extending the exposure time. This, of course, also reduces the frame rate to non-standard values.

Automatic exposure and gain control are enabled with AEC=1 (pin 21) and AGC=1 (pin 22), but can be inhibited via the serial interface (Setup Code_1). However, If AEC is inhibited by pin 21, AGC is also inhibited and the serial interface has no control. Inhibiting AEC or AGC via the serial interface, or by taking pin 21 or 22 low, freezes the current value(s) for these, which can then be altered by writing to the exposure and gain control registers. (See Serial Interface for details.)

Note: The timing of exposure and gain control messages on the serial interface is very important. External values for exposure and gain are only applied at the start of a frame, and the serial interface must be paused until the new values are installed—no further communications will be accepted during this time.

Automatic Exposure Control (AEC)

Automatic exposure control is achieved by varying pixel current integration time according to the average light level on the sensor. This integration time can vary from one pixel clock period to one frame period.

Pixels above a threshold white level are counted every frame, and the number at the end of the frame defines the image as overexposed, above average, correctly exposed, below average or underexposed. If the image is other than correctly exposed, a new value for integration time is calculated and applied for the next frame. Corrections are either ±1/8 or ±1/64, depending upon the degree of over or under exposure. If the exposure value is close to its limit (12% below max. or 25% above min.), then gain is increased or decreased by one step and exposure is set to midway in its range. Exposure is then controlled as normal.

Automatic Gain Control (AGC)

The VV5430 automatically increases the system gain of its output stage if with the current gain setting and maximum exposure the image is too dark. Gain can be varied from x1 to x16 in times-two steps, giving five different gain settings.

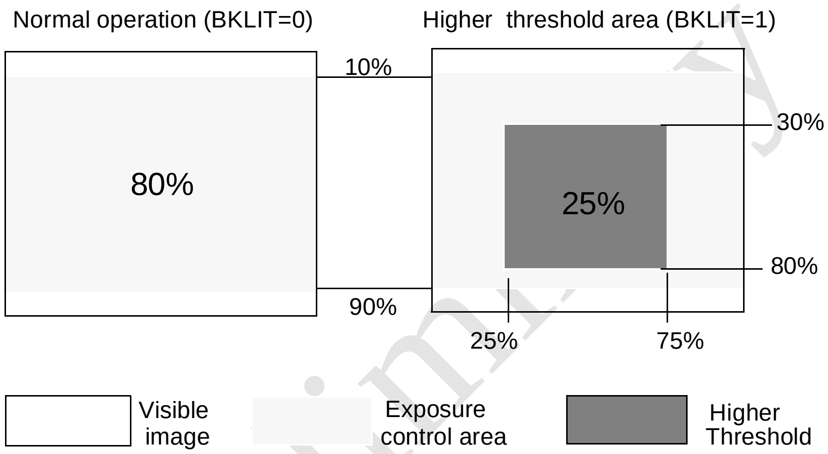
If the scene is too dark and the integration period has almost reached its maximum value, the gain value is incremented by one step (times two). In the same frame period the exposure value is divided by two, halving the integration period. The exposure controller then increases the exposure value as necessary. Similarly if the image is too bright and the integration period is short then gain will be reduced by one step (divide by two) and the exposure value will be doubled. The exposure controller can then adjust the exposure value as necessary to provide a correctly exposed image.

Increasing gain is limited to a programmable upper limit, for which the default value is x8. The gain upper limit is programmed by setting bits [0..3] with header code 0101, when AGC=1. If Automatic Gain Control is inhibited (AGC=0), these registers are used instead to select a gain setting up to x16.

Backlit Mode

The VL5430 can be configured to operate in two auto-exposure modes, selected by the BKLIT option via the serial interface (Setup Code_1, bit 0). The default mode (BKLIT = 0) provides exposure control for normally illuminated scenes. For scenes where a bright background can cause the foreground subject to be severely under exposed, the ‘Backlit’ mode (BKLIT = 1) offers superior performance.

‘Backlit Mode’ (BKLIT=1) operates by using a higher threshold level for the exposure control comparator over the central area of an image, which is therefore exposed for longer and so enhanced. The area in which the higher comparator threshold is used when BKLIT=1 is illustrated below:



Note: The threshold level used for the central area is a preset mutiple of the normal mode reference level, and is not alterable.

SERIAL COMMUNICATION

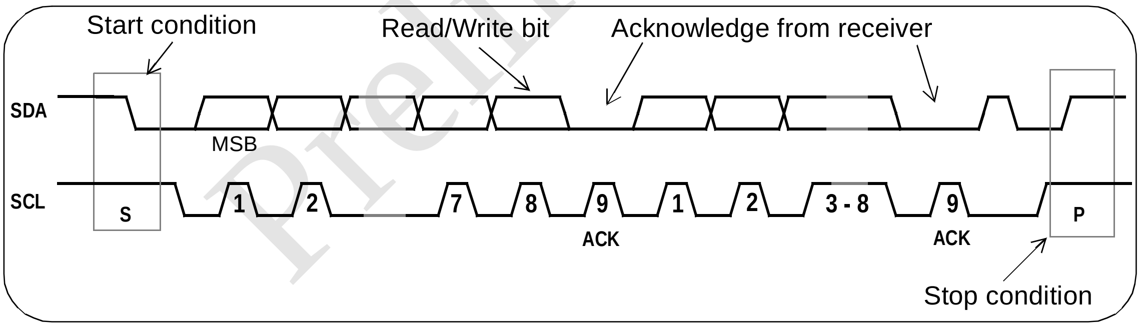
The VL5430 includes a full duplex (two-wire) serial interface, and can be controlled and configured by a host processor. The base bus address for the VL5430 is 20_H, but the two least significant bits of the address (SAB0, SAB1) can be selected by linking pins 20 and/or 16 to VDD. This allows up to four separate camera devices to be controlled on one serial link, which, for example, makes multiplexing of camera outputs possible.

The serial interface reads or writes data to a set of Registers that define the characterisation of the sensor, and control certain operations.

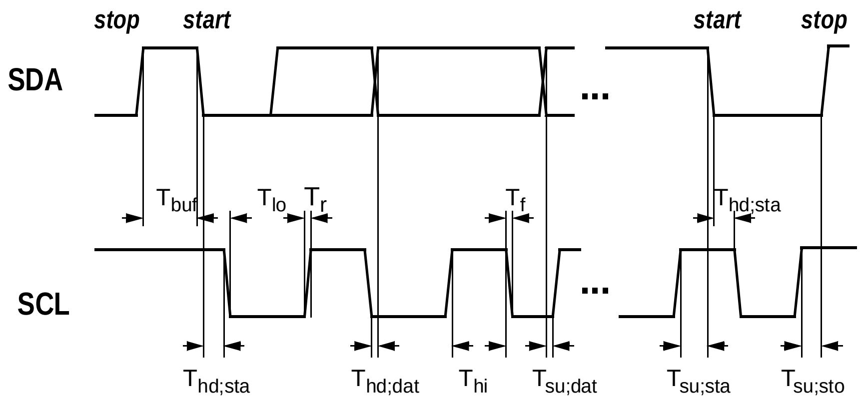
Serial Communication Protocol

The host must perform the role of a communications master and the camera acts as either a slave receiver or transmitters communication between host and camera takes the form of three or five byte messages of 8-bit data, with a maximum serial clock (SCL) frequency of 100kHz. Since the serial clock is generated by the host, the host determines the data transfer rate.

The host processor initiates a message by forcing both Serial Data (SDA) and Serial Clock (SCL) low. The first byte addresses the required device, and defines either a READ message (four bytes to follow) or a WRITE message (two bytes to follow). After the camera has acknowledged a valid address (ACK, bit 9 of SCL), the host then either reads four bytes of data from the camera or transmits a further two bytes to the camera. The data transfer protocol on the bus is illustrated below:



Data Transfer Protocol



Note: All values referred to the minimum input level (high) = 3.5V, and maximum input level (low) = 1.5V

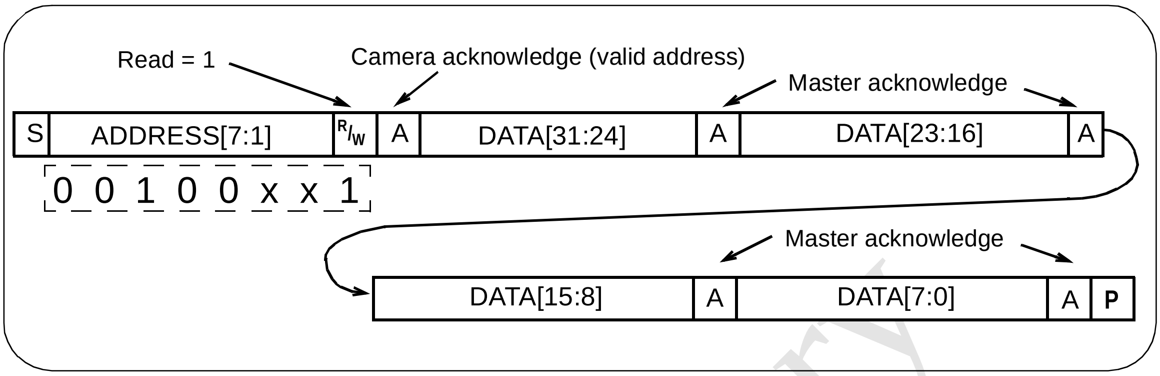
Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	F_{scl}	0	100	kHz
Bus free time between a stop and a start	T_{buf}	4.7	-	µs
Hold time for a repeated start	$T_{hd;sta}$	4.0	-	µs
LOW period of SCL	T_{lo}	4.7	-	µs
HIGH period of SCL	T_{hi}	4.0	-	µs
Set-up time for a repeated start	$T_{su;sta}$	4.7	-	µs
Data hold time	$T_{hd;dat}$	0[1]	-	µs
Data Set-up time	$T_{su;dat}$	250	-	ns
Rise time of SCL, SDA	T_r	-	1000	ns
Fall time of SCL, SDA	T_f	-	300	ns
Set-up time for a stop	$T_{su;sto}$	4.0	-	µs
Capacitive load of each bus line (SCL, SDA)	C_b	-	100	pF

1. The VV5430 internally provides a hold time of at least 300ns for the SDA signal (referred to the minimum input level (high) of the SCL signal) to bridge the undefined region of the falling edge of SCL

Serial Interface Timing Characteristics

READ DATA FROM CAMERA

Information describing the current configuration and the current exposure values can be read from the camera. The data is formed into four bytes of 8 bits. Each pair of bytes is considered to be a data word and is read out msb first.



Read Data Format

The following tables defines the information contained in the read messages. By default, the Primary Read Data is accessed; only if a Secondary Read Select bit is set in Setup Code_2 (header code 0010) is the Secondary information read.

Primary Read Data:

Bit	Function
31 - 23	Coarse Exposure Value (9 bits)
22 - 14	Fine Exposure Value (9 bits)
13 - 10	Gain Value (4 bits)
9	Auto Exposure Control on/off
8	Internal Black Calibration on/off
7	Auto Gain Control on/off
6	Gamma or Linear Video Output
5	Normal or Backlit mode[1]
4	Undefined
3 - 0	Camera Type ID Code (4 bits)

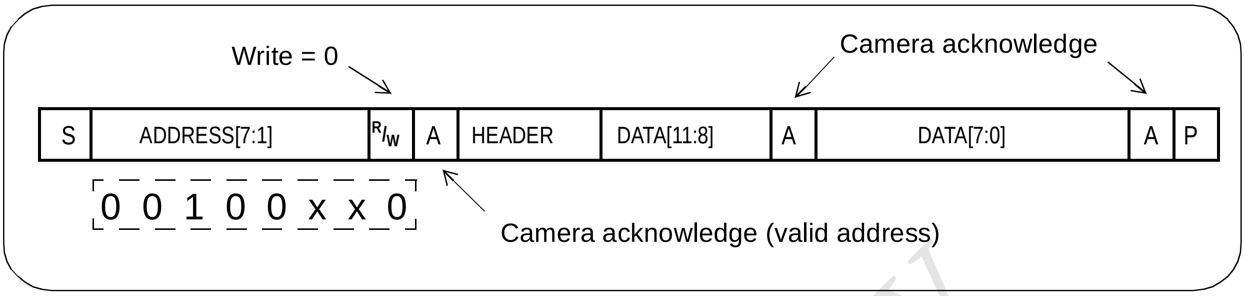
1. Bit 5 of the Primary Read message only reflects the state of the BKLIT pin, not the combined result of the pin and the serial interface BKLIT control bit.

Secondary Read Data:

Bit	Function
31 - 18	Undefined
17	Black Level monitor in progress
16 - 0	White Pixel count (17 bits)

WRITE TO CAMERA

Information to be communicated from host to camera consists of configuration data (for example automatic gain control ON), and parametric information (for example sensor integration time). The write data is formed into two bytes. A 4-bit Header Code in the first byte is used by the camera to determine the destination of the 12-bit message following the header.



Receive Data Format

After the camera acknowledges the receipt of a valid address the host transfers the first data byte which the camera acknowledges by pulling SDA low. The second byte is then sent followed by a final acknowledge from the camera. A stop condition is produced by the host after the second message byte. As with the read procedure, the stop condition is not absolutely necessary as the camera's serial interface will reset automatically after two bytes have been received.

The valid Header Codes and their data structures are fully described in the following pages.

Timing Protocol

When an exposure or gain value has been written to the camera it is held in the interface until the camera is ready to consume the new data. For correct operation, there should be no further read or write accesses to the camera during this hold period. Normal communication between other modules connected to the serial interface will not cause problems. The minimum length of the wait period is **40ms** in EIA mode and **34ms** in CCIR mode from the end of the data transfer.

Header Codes

The message can be a configuration word, an exposure, gain or calibration value. The camera's interpretation of the header code and the set-up code message are given in the table below. Defaults for each control bit are built in to the camera's reset cycle, and may be changed on-the-fly under host control.

Code	Interpretation	Comment
0000	Invalid	
0001	Set-up code_1 (9 bits)	Basic funtionality options
0010	Set-up code_2 (9 bits)	Pixel control & Read Data
0011	Coarse exposure value (9 bits)	Set AEC=0 to enable
0100	Fine exposure value (9 bits)	Set AEC=0 to enable
0101	Gain control value (4 bits)	Set AGC=0 to enable
0110	Unused	
0111	Unused	
1000	Exposure control T1 threshold (9 bit)	
1001	Exposure control T2 threshold (9 bit)	
1010	Analogue control register (8 bit)	
1011	Reserved	Not applicable to normal use
1100	Reserved	Not applicable to normal use
1101	Reserved	Not applicable to normal use
1110	Set-up code_3 (6 bits)	Pixel synchronisation
1111	Test mode select	Not applicable to normal use

Header Codes

Message content

The following Tables contain details of the data associated with each header code, and the number of valid data bits in each of the registers. In all cases the full 12 bit message tail can be sent, the valid bits being packed to the lsb. (Normally, the unused bits would be assigned zeroes.)

Setup Code_1

Header Code = 0001 **Valid data bits: 11**

The code_1 setup register is used to select different basic operating modes:

Bit	Function	Default	Comment
0	Normal/Backlit	0	Selects between normal and backlit exposure modes. The power-on default is normal mode. See Exposure Control for full description
1	Linear Correction enable	0	Selects between a linear (LIN=1) or gamma corrected video signal on AVO. The power-on default is gamma corrected.
2	Auto gain control enable	1	Allows automatic gain control to be inhibited. The current gain value selected is frozen. With AGC=0 a new gain value can be written to the gain register via the serial interface (header code 0101).
3	Inhibit black calibration	0	Allows automatic black calibration to be inhibited.
4	Auto exposure control enable	1	Allows automatic exposure control to be inhibited. The current exposure value selected is frozen. Note that if automatic exposure control is inhibited then automatic gain control is also disabled. With AEC=0 a new exposure value can be selected by writing to the coarse and fine exposure registers via the serial interface (header codes 0011 & 0100).
5	Horizontal shuffle enable	0	Shuffles the read out of the horizontal shift register. Even columns read out together then odd columns.
6	Vertical shuffle enable	0	Shuffles the readout of the vertical shift register. Even lines read out together then odd lines.
7	Force black calibration	1	Requests a re-calibration of the black level while bit is low.
8	Clock divisor DIV0	0	System clock division: (see Note) 0,0=1; 0,1=÷2; 1,0=÷4; 1,1=÷8
9	Clock divisor DIV1	0	
10	Internal Register	1	This bit must be set(=1) for correct sensor operation
11	Not used	0	

Set-up code_1

Note: Decreasing the system clock rate proportionately increases sensor sensitivity (by increasing exposure time), but also decreases frame frequency. System Clock must be x1 for standard CCIR or EIA framing.

Setup Code_2

Header Code = 0010 **Valid data bits: 12**

The code_2 setup register is used to select read data, valid pixels and video output operating modes:

Bit	Function	Default	Comment
0	Shadow read mode (A) enable	0	Select shadow read mode A or B. Note: bits 0,1 are mutually exclusive.
1	Shadow read mode (B) enable	0	
2	Pixel sample clock select (SEL0)	CPE	Pixel sample clock mode (PV/PVB). See below.
3	Pixel sample clock select (SEL1)	0	
4	Not used	0	MUST be set to 0
5	Enable free running pixel clock	0	Overrides SEL0 & SEL1.
6	Enable external pixel thresholds	0	Use external algorithm thresholds in exposure controller
7	Not used	0	MUST be set to 0
8	Not used	0	MUST be set to 0
9	OE[0]	0	AVO output enable control bits [0..2]. See Shuffle Modes above for explanation.
10	OE[1]	0	
11	OE[2]	0	

Setup Code_2

The table below shows the function of SEL0 and SEL1 (Bit 2 and Bit 3); the default value of SEL0 is set by the CPE pin level:

Bit 3	Bit 2	Pixel Clock (PV/PVB pins) function
0	0	Disable pixel clock output
0	1	Qualify full image area (as defined for CCIR or EIA)
1	0	Qualify central 256 x 256 pixels (CCIR only)
1	1	PV/PVB active only during interline periods of visible image lines. Note. This mode is required for digitisation of standard video output.

Coarse and Fine Exposure Values.

Header Code (coarse) = 0011 Valid data bits: 9

Header Code (fine) = 0100 Valid data bits: 9

The 18 bit exposure control value is formed from two 9-bit values, coarse (9 msb's) and fine (9 lsb's). For external exposure control (AEC = 0) the exposure value can be set via the serial interface (header codes 0011 and 0100). Values written that exceed the mode dependant maxima will be ignored and the maximum will be used.

Bit	Function	CCIR		EIA		Comments
		min	max	min	max	
0-8	Coarse exposure value	0	310	0	260	Header code 0011
0-8	Fine exposure value	0	404	0	325	Header code 0100
9-11	Unused					

Exposure Values

Exposure Control Thresholds T1 and T2

Header Code (T1) = 1000 Valid data bits: 9

Header Code (T2) = 1001 Valid data bits: 9

The lower and upper pixel count thresholds are used by the automatic exposure controller. The power-on default values for T1 and T2 are exposure mode and video mode dependant. If the external pixel threshold control bit (bit 6 in Setup Code_2 register) is set the internal default values for T1 and T2 are overridden by the serial interface values. Note that only the most significant nine bits of each seventeen bit threshold can be controlled.

Bit	DAC	Comments
0 - 8	Lower Exposure control threshold (T1)	Header Code 1000
0 - 8	Upper Exposure control threshold (T2)	Header Code 1001
9 - 11	Unused	

Pixel Count Thresholds (T1,T2)

Gain and Gain Ceiling

Header Code = 0101 **Valid data bits: 4**

This register is used to select an external gain value when automatic gain control is inhibited (AGC = 0) and to set the gain ceiling while automatic gain control is active (AGC = 1).

Bit	Function	Default	Comment
0	Gain value G[0]	0	Default gain value
1	Gain value G[1]	0	
2	Gain value G[2]	0	
3	Gain Value G[3]	0	Default gain ceiling
4-11	Unused		

Gain Register

The table below shows the valid gain codes.

G[3]	G[2]	G[1]	G[0]	Gain	Comment
0	0	0	0	1	Default gain value
0	0	0	1	2	
0	0	1	1	4	
0	1	1	1	8	Default gain ceiling
1	1	1	1	16	

Gain Values

Analogue Control Register

Header Code = 1010 **Valid data bits: 10**

A number of parameters that are used to define internal operations can be altered by the serial interface:

Bit	Function	Default	Comments
0	Internal	1	Must be set(=1) for normal op.
1	Internal	0	Must be 0 for normal op.
2	Internal	0	Must be 0 for normal op.
3	Disable anti-blooming protection	0	
4	Internal	0	Must be 0 for normal op.
5	Internal	0	Must be 0 for normal op.
6	Enable external black reference	0	
7	Enable external white threshold	0	
8	Internal	0	Must be 0 for normal op.
9	Enable binarisation of AVO output	0	AVO output level is either V_{BLACK} or V_{WHITE} for each pixel (see Note)l

Control Register

Note: The Threshold Level above which a pixel is deemed to be WHITE is set via the serial interface, Header Codes 1001 and 1000 (Upper and Lower Exposure Control Thresholds).

Setup Code_3

Header Code = 1110 **Valid data bits: 7**

This register stores data used during sensor synchronisation and when the pixel counter in the video timing logic is reset, either at the end of a video line or when the sensor is forced to synchronise externally.

Bit	Function	Default	Comment
5:0	Video timing pixel counter offset	3	Variable offset that is added to the fixed pixel counter preset value when the counter is reset, at the end of a video line or when an external synchronisation is applied
6	Enable SNO	0	Synchronising signal to other cameras in multi-camera applications (see Note)
11:7	Not used	0	

Set-Up Code_3

Note: Enable SNO adjusts the timing of the FST signal (output on pin 36) to correctly synchronise external slave cameras. Alternatively, the synchronising signal for all cameras can be generated externally, which may be more useful in image processing applications.

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