Original

DWG.NO.	SH 1	REV.

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

VCC

TX Pad 22

RX Pad 21

MAX203 U3 SOIC

T1OUT T2OUT R1IN R2IN C2a+ C2b+ C2a- C2b- GND2 GND1 T1IN T2IN R1OUT R2OUT Va- Vb- MAX203

C1 0.1uF C2 0.1uF

CLK

DATA

LDA Pad 9

LCL Pad 10

U4 SO8 82B715SX LX LY GND SY

C3 0.1uF C4 0.1uF C20 0.01uF

Pad 13 DIG_IO2_I_TIMER1_IN

Pad 11 DIG_IO3_I_PWM2

DIG_IO4_I_PWM1 Pad 12

AD_CSn DA_CSn AD_SHDNn DA_SHDNn DIN_EN

DIG_IO0_I_TIMER0_IN Pad 14

DIG_IO1_I_INT Pad 20

DOUT_EN

Pad 19 DIG_IO5

Pad 18 DIG_IO6

Pad 17 DIG_IO7

Pad 16 DIG_IO8

Pad 15 DIG_IO9

PIC16C65A U1 PLCC

RA0 RA1 RA2 RA3 RA4_TOCKI RA5_SSn RB0_INT RB1 RB2 RB3 RB4 RB5 RB6 RB7 OSC1_CLKIN OSC2_CLKOUT MCLRn_VPP RC0_T1OSO_TICKI RC1_T1OSI_CCP2 RC2_CCP1 RC3_SCK_SCL RC4_SDI_SDA RC5_SDO RC6_TX_CK RC7_RX_DT RD0_PSP0 RD1_PSP1 RD2_PSP2 RD3_PSP3 RD4_PSP4 RD5_PSP5 RD6_PSP6 RD7_PSP7 RE0_RDn RE1_WRn RE2_CSn VCC1 VCC2 GND1 GND2 GND3

PORn

VCC

C5 0.1uF

ECS-16 U5 SOIC ECS-16 SEL2 SEL1 SEL0 EN GND VCC 16MHZ DIV

P1 PAD PAD P3 PAD P2

16MHz

2MHz

74AC139 U11 BIN/Y EN

74AC14 U9

POR

RESETn

VCC1 VCC2 GND

CHA Pad 24

CHB Pad 25

PULSE

SIGN

LIMITn Pad 32

STOPn Pad 31

PROF Pad 33

INIT

INDEX Pad 30

PHA Pad 29

PHB Pad 28

PHC Pad 27

PHD Pad 26

HCTL1100 U2 PLCC

AD0 AD1 AD2 AD3 AD4 AD5 D6 D7 ALEn CSn OEn R_Wn EXTCLK SYNCn RESETn MC0 MC1 MC2 MC3 MC4 MC5 MC6 MC7 GND1 GND2 GND3

REV. A	SIZE D	FSCM NO.	DWG.NO.	REV.
DRAWN newell				
ISSUED	SCALE		SHEET 1 OF XX	

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Design Pathname	Version	Edited By	Last Edit
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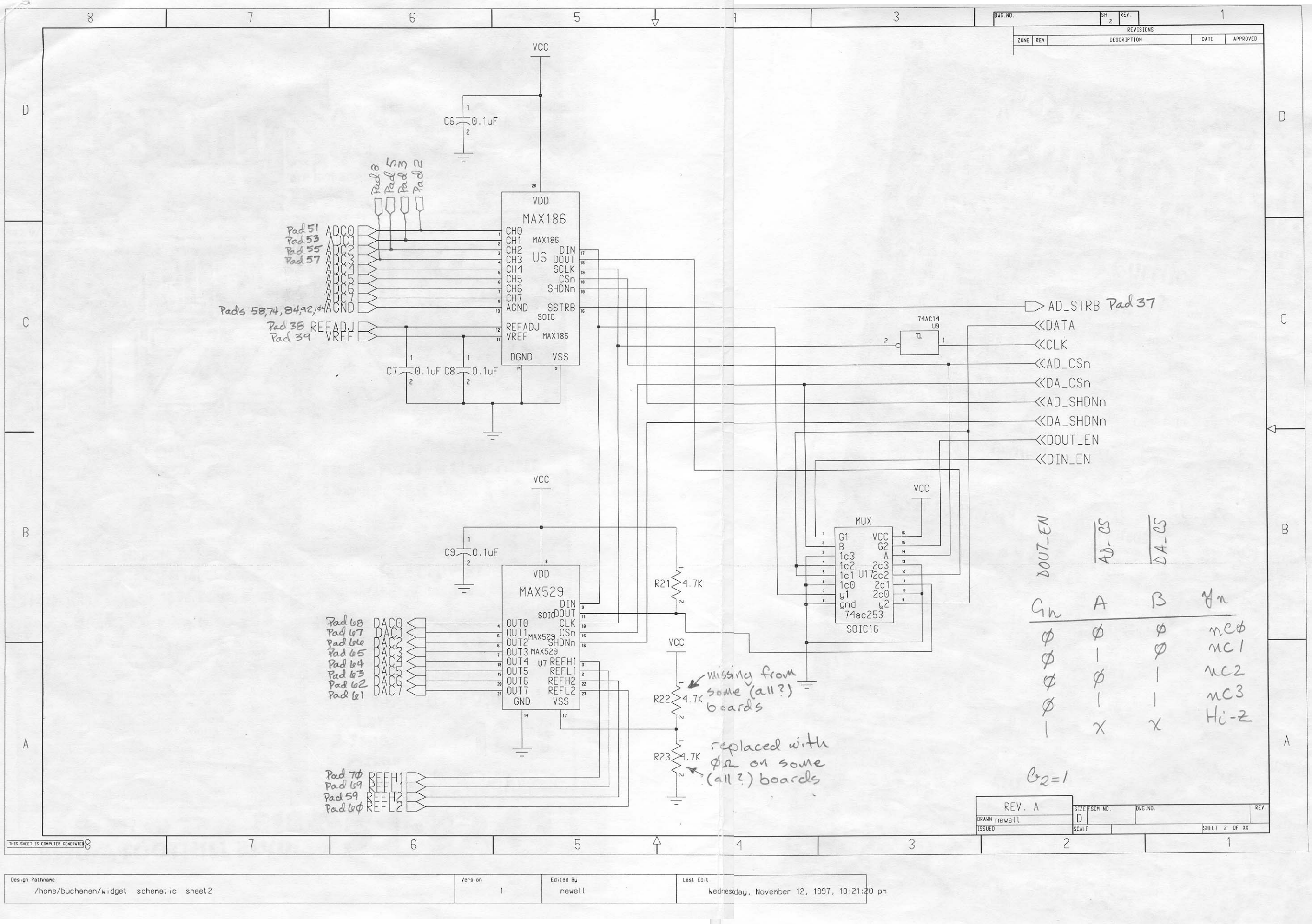
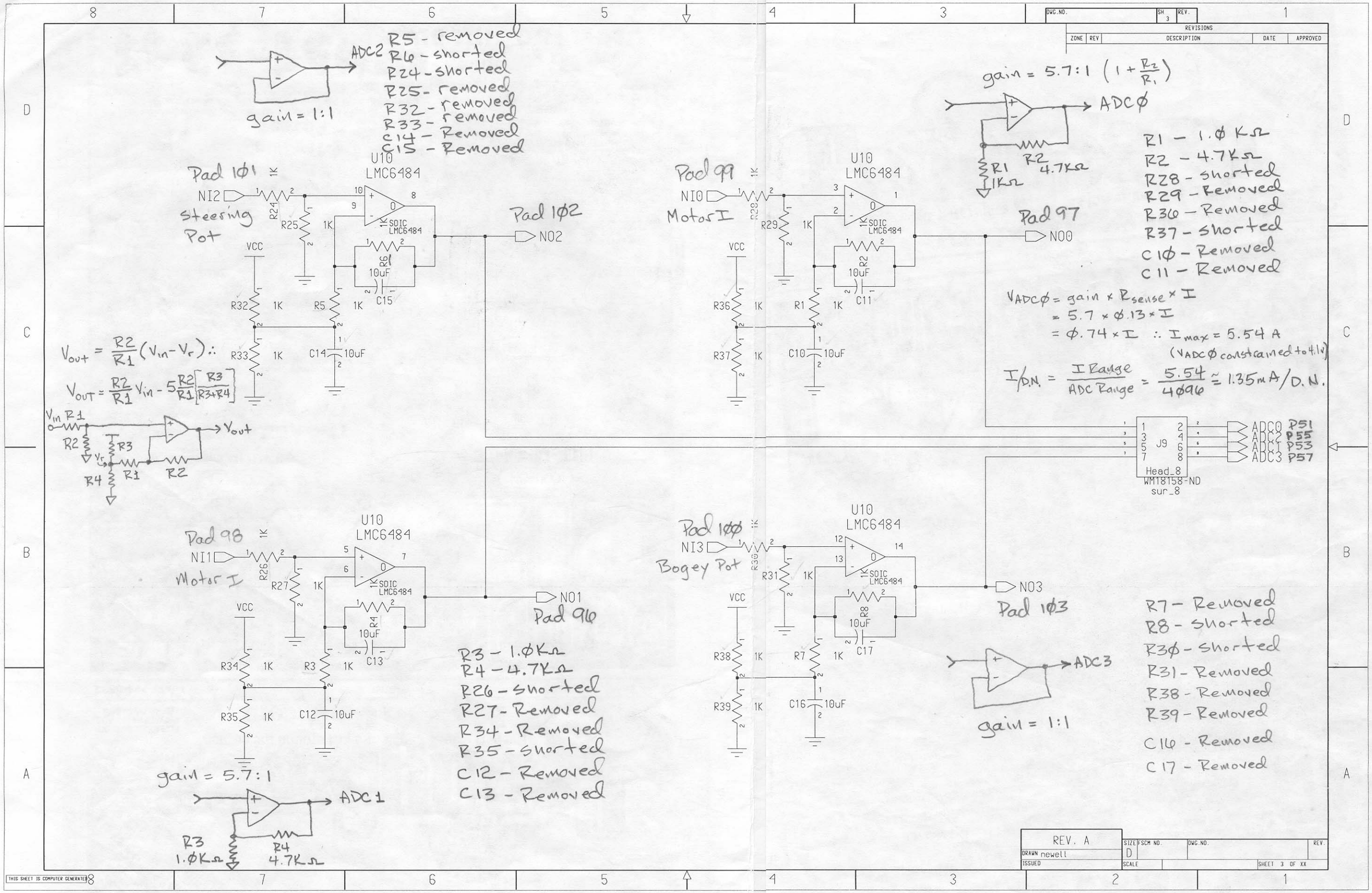
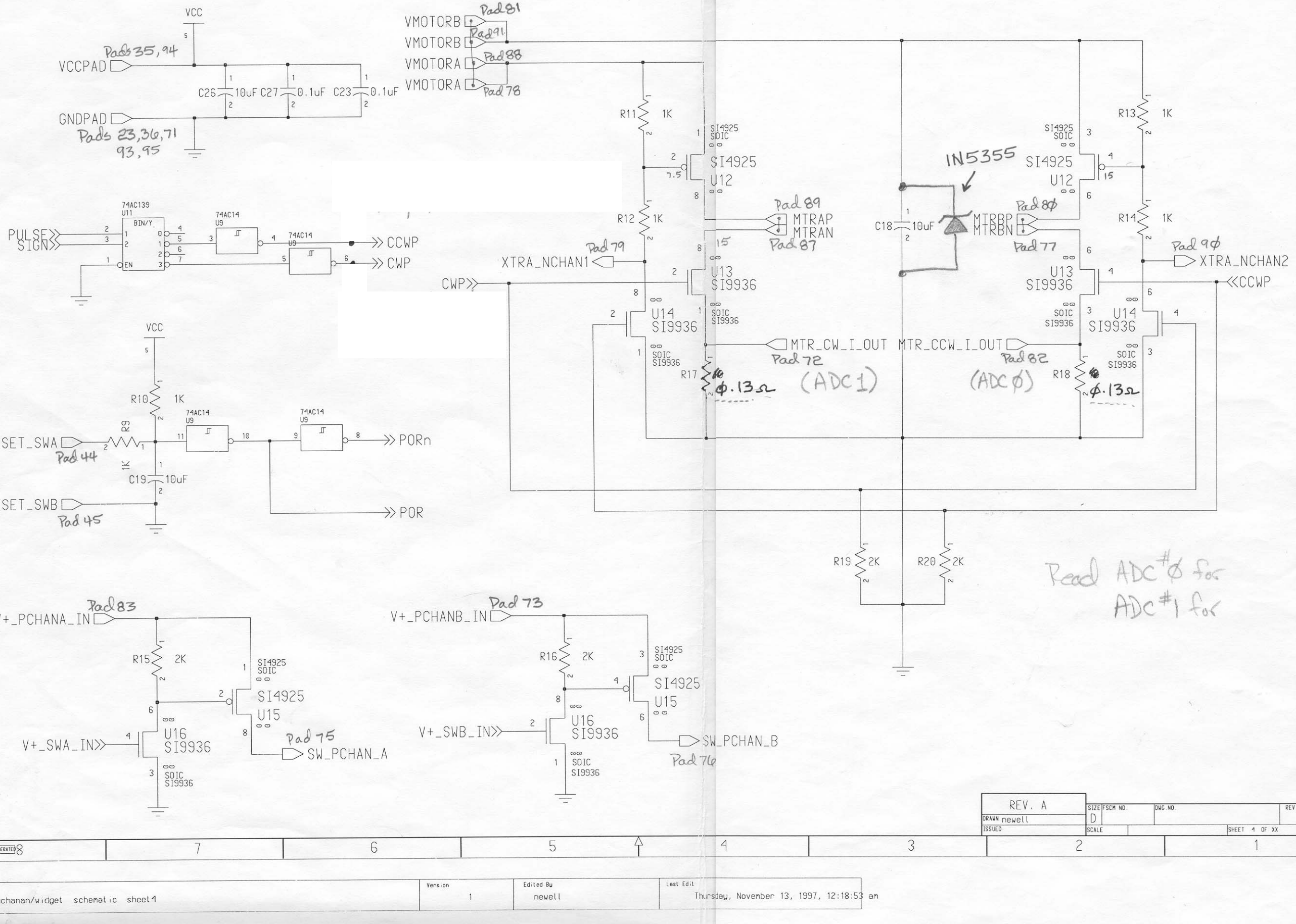


Design Pathname	Version	Edited By	Last Edit
/home/buchanan/widget schematic sheet2	1	newell	Wednesday, November 12, 1997, 10:21:20 pm



Design Pathname	Version	Edited By	Last Edit
/home/buchanan/widget schematic sheet3	1	newell	Wednesday, November 12, 1997, 11:49:29 pm


VCC
Pads 35,94
VCCPAD
GNDPAD
Pads 23,36,71 93,95
C26 10uF
C27 0.1uF
C23 0.1uF
VMOTORB Pad 81
VMOTORB Pad 91
VMOTORA Pad 88
VMOTORA Pad 78
R11 1K
R12 1K
SI4925 SOIC
SI4925 U12
Pad 89 MTRAP
Pad 87 MTRAN
Pad 79 XTRA_NCHAN1
CWP
U13 SI9936
U14 SI9936
SOIC SI9936
MTR_CW_I_OUT
Pad 72
R17 .13Ω
(ADC1)
IN5355
C18 10uF
Pad 80 MTRBP
MTRBN Pad 77
R13 1K
R14 1K
Pad 90 XTRA_NCHAN2
CCWP
MTR_CCW_I_OUT
Pad 82
R18 .13Ω
(ADC0)
74AC139 U11
BIN/Y
EN
PULSE
SIGN
74AC14 U9
CCWP
CWP
R10 1K
R9 1K
RESET_SWA Pad 44
C19 10uF
RESET_SWB Pad 45
PORn
POR
R19 2K
R20 2K
Read ADC#0 for
ADC#1 for
V+_PCHANA_IN Pad 83
R15 2K
U16 SI9936
V+_SWA_IN
Pad 75 SW_PCHAN_A
V+_PCHANB_IN Pad 73
R16 2K
V+_SWB_IN
SW_PCHAN_B
Pad 76
REV. A
DRAWN newell
ISSUED
SIZE D
SCALE
SHEET 1 OF XX
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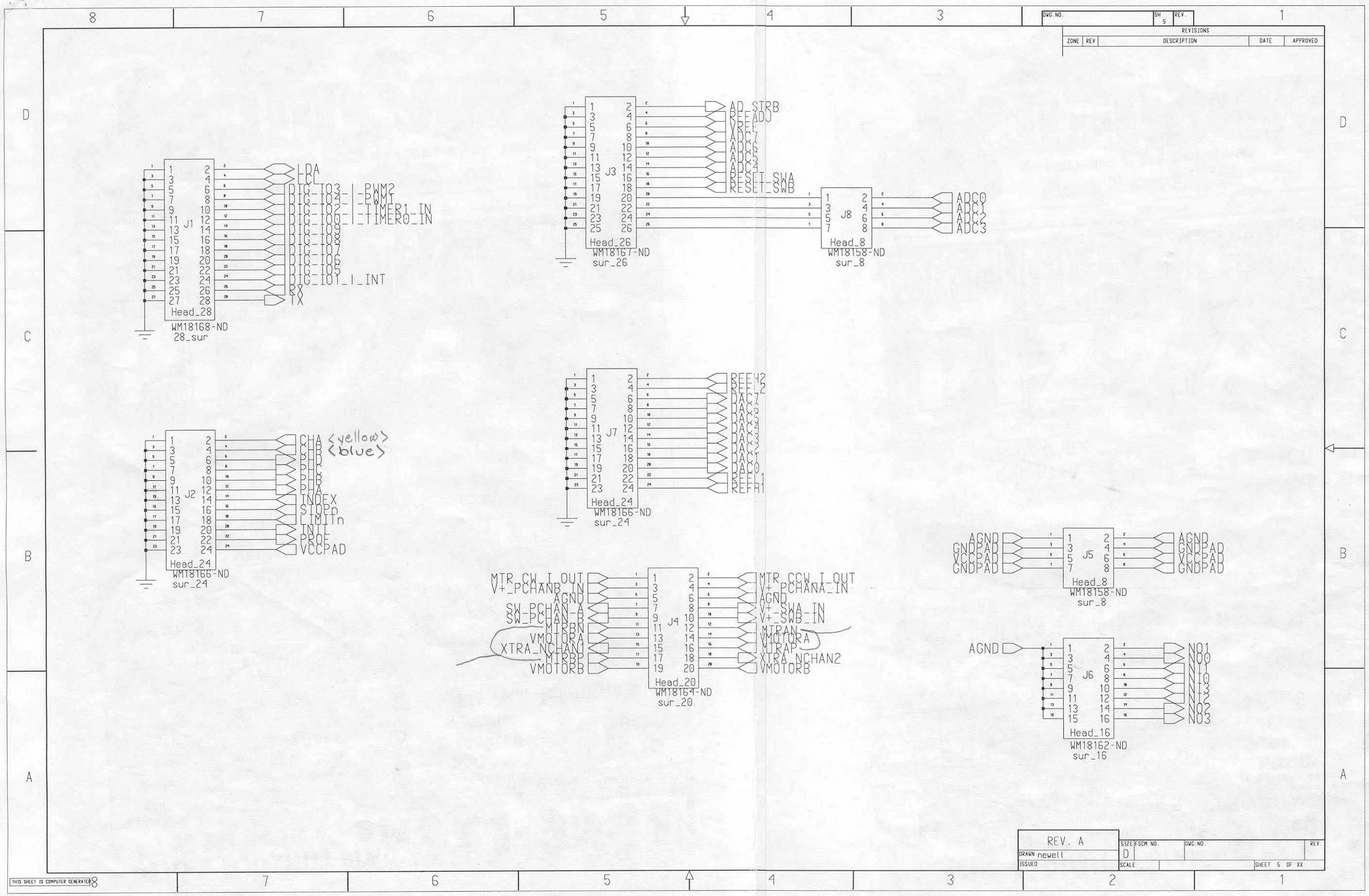
Design Pathname
/home/buchanan/widget schematic sheet1
Version 1
Edited By newell
Last Edit Thursday, November 13, 1997, 12:18:53 am

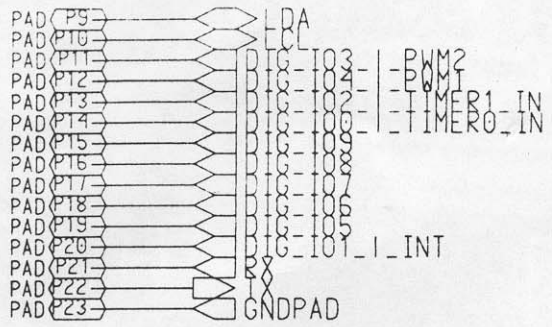


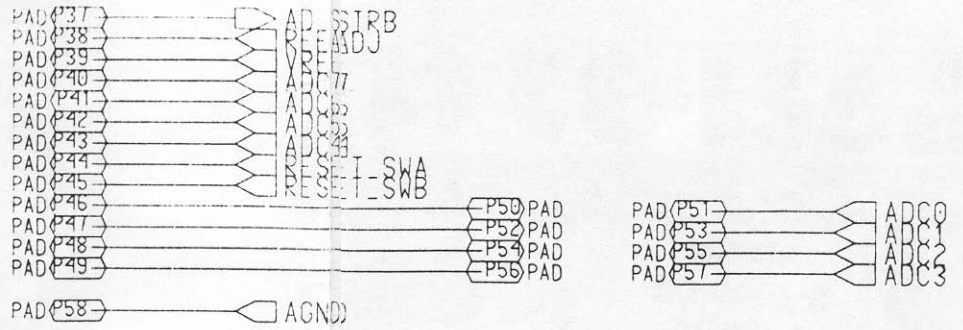
Design Pathname	Version	Edited By	Last Edit
/home/buchanan/widget schematic sheet5	1	newell'	Friday, January 30, 1998, 1:30:21 pm

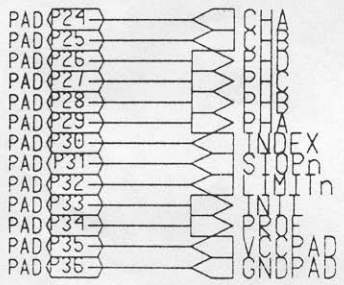
DWG NO	SH 5	REV

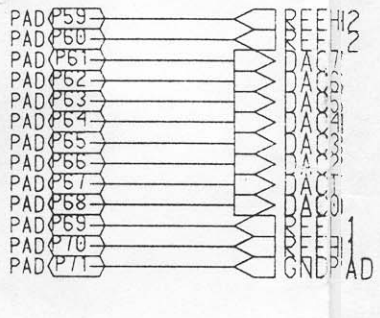
REVISIONS

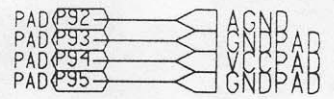
ZONE	REV	DESCRIPTION	DATE	APPROVED



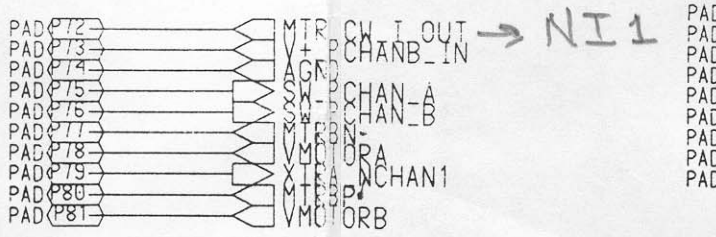


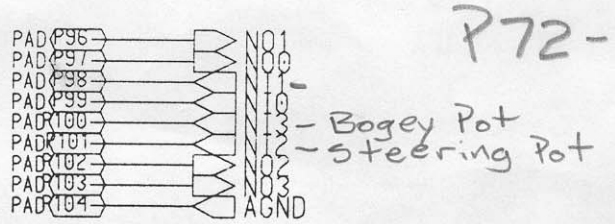






P82- P99 IAN
~~P101-P82~~
P92-P71
P72-98





Compact Widget Board

REV A	SIZE D	SCH NO	DWG NO	REV
DRAWN newell				
ISSUED	SCALE		SHEET 5 OF 9	

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Design Pathname	Version	Edited By	Last Plot
/home/buchanan/w4/comp/schematic/sheet5	14	buchanan	Fri Mar 19, 1999, 8:47:28 am

5-10-99